IN THE CLAIMS:

1. (Currently Amended) A delay circuit comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; and

selecting switch sections, wherein

at least one of the selecting switch sections ~~comprise~~ comprises:

a buffer section for receiving delayed input signal from one of the delay stages; and

a selecting section means directly connected to the buffer section for activating the buffer section to establish ~~the~~ a delay path, wherein

an output signal from the delay path has a desired delay time.

2. (Previously Amended) The delay circuit according to claim 1, wherein at least one of the predetermined delay stages is provided with an individual delayed output terminal for outputting an individual delayed output signal having an individual predetermined delay time, and wherein at least one selecting switch section is provided for each individual delayed output terminal with an input terminal of the buffer section being connected to the individual delayed output terminal and output terminals of the selecting switch sections being mutually joined.

Claim 3 (canceled)

4. (Currently Amended) The delay circuit according to claim 1, wherein, the buffer section is provided with a first transistor whose gate terminal is set as an input terminal, and the selecting section means is provided with a second transistor into whose gate terminal a control signal for establishing the delay path in the delay section is input, and the first and second transistors are connected directly in series between the output terminal of the selecting switch section and a first power supply voltage.

5. (Previously Amended) The delay circuit according to claim 4, wherein the first transistor is connected between the second transistor and the output terminal.

6. (Previously Amended) The delay circuit according to claim 4, wherein the first transistor is connected between the second transistor and the first power supply voltage.

7. (Currently Amended) The delay circuit according to claim 4, wherein the buffer section further comprises a third transistor whose gate terminal is connected to the input terminal, and the selecting section means further comprises a fourth transistor into whose gate terminal the control signal for establishing the delay path in the delay section is input, and the third and fourth transistors are connected directly in series between the output terminal of the selecting switch section and a second power supply voltage.

8. (Previously Amended) The delay circuit according to claim 7, wherein the first transistor is connected between the second transistor and the output terminal of the selecting switch section and the third transistor is connected between the fourth transistor and the output terminal.

9. (Previously Amended) The delay circuit according to claim 7, wherein the second transistor is connected between the first transistor and the output terminal of the selecting switch section and the fourth transistor is connected between the third transistor and the output terminal.

10. (Original) The delay circuit according to claim 4, wherein the first power supply voltage is a power supply voltage potential and the first and second transistors are PMOS transistors.

11. (Original) The delay circuit according to claim 4, wherein the first power supply voltage is a ground potential and the first and second transistors are NMOS transistors.

12. (Original) The delay circuit according to claim 7, wherein the second power supply voltage is a power supply voltage potential and the third and fourth transistors are PMOS transistors.

13. (Original) The delay circuit according to claim 7, wherein the second power supply voltage is a ground potential and the third and fourth transistors are NMOS transistors.

14. (Previously Amended) The delay circuit according to claim 4, wherein drive capacity of the second transistor is larger than drive capacity of the first transistor.

15. (Previously Amended) The delay circuit according to claim 7, wherein drive capacity of the fourth transistor is larger than drive capacity of the third transistor.

16. (Previously Amended) The delay circuit according to claim 2, wherein, in the delay section, the individual delayed output terminal is connected to an input terminal of the next one of the predetermined delay stages and a plurality of the predetermined delay stages are connected in series.

17. (Currently Amended) The delay circuit according to claim ~~3~~ 32, wherein, in the delay section, the output terminal of each of the predetermined delay stages is connected to the individual delayed input terminal of the next one of the predetermined delay stages and a plurality of the predetermined delay stages are connected in series.

18. (Previously Amended) The delay circuit according to claim 16, wherein, in at least one of the predetermined delay stages, the rise delay time and fall delay time for a signal inputted to each of the predetermined delay stages are substantially uniform.

19. (Previously Amended) The delay circuit according to claim 18, wherein each of the predetermined delay stages comprise an even number of logic inversion sections connected in series, in which the rise delay time and fall delay time for the signal are substantially uniform.

20. (Original) The delay circuit according to claim 19, wherein the logic inversion sections are inverter gates.

21. (Previously Amended) The delay circuit according to claim 16, wherein each of the predetermined delay stage comprises an even number of logic inversion sections connected in series, in which the rise delay time and fall delay time of the signal are different.

22. (Previously Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NAND gate that forms inverted logic through input terminals other than the input terminal into which the signal is input being connected to a power supply voltage potential.

23. (Previously Amended) The delay circuit according to claim 21, wherein each of the logic inversion sections is a NOR gate that forms inverted logic through input terminals other than the input terminal into which the signal is input being connected to a ground potential.

24. (Original) The delay circuit according to claim 16, wherein the delay section is formed from predetermined delay stages each having the same structure.

25. (Previously Amended) The delay circuit according to claim 4, wherein, when the delay path in the delay section is established using two or more control signals,

there is provided instead of the second transistor, two or more transistors connected in series into whose respective gate terminals the respective control signals are input.

26. (Currently Amended) A semiconductor integrated circuit device comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; and

selecting switch sections, wherein

at least one of the selecting switch sections ~~comprise~~ comprises:

a buffer section for receiving delayed input signal from one of the delay stages; and

a selecting section means directly connected to the buffer section for activating the buffer section to establish ~~the~~ a delay path, wherein

an output signal from the delay path has a desired delay time.

27. (Currently Amended) The semiconductor integrated circuit device according to claim 26, wherein, the buffer section is provided with a first transistor whose gate terminal is set as an input terminal, and the selecting section means is provided with a second transistor into whose gate a terminal control signal for establishing the delay path in the delay section is input, and the first and second transistors are connected directly in series between the output terminal of the selecting switch section and a first power supply voltage.

28. (Previously Amended) The semiconductor integrated circuit device according to claim 26, wherein, in at least one of the predetermined delay stages, the rise delay time and fall delay time for a signal inputted to each of the predetermined delay stages are substantially uniform.

29. (Previously Amended) A delay method comprising:

a delay step in which predetermined delay times are sequentially added onto an input signal to obtain delay signals;

a selecting step for obtaining one of the delay signals in the delay step which has a desired delay time; and

an output step in which one of the delay signals in the delay step is output by activating the selecting step.

30. (Original) The delay method according to claim 29, wherein the selecting step includes a step in which the required power is supplied to the output step.

31. (Previously Amended) The delay method according to claim 29, wherein, in the delay step, each of the predetermined delay times has a substantially uniform delay time between rising time and falling time of a signal inputted to.

32. (Currently Amended) A delay circuit comprising:

a delay section having two or more predetermined delay stages each of which is provided with an individual delay input terminal for inputting a signal to which

predetermined delay time is added, the signal inputted to each predetermined delay stage having substantially uniform rise delay time and fall delay time, and

selecting switch means connected to the delay section for establishing ~~the~~ a delay path for the input signal by selecting one of the delay stages,

wherein an output signal from the delay path has a desired delay time.

33. (New) A delay circuit comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; and

selecting switch sections, at least one of the selecting switch sections comprises:

a buffer section, the buffer section comprises a first transistor, a gate of the first transistor receiving a delayed input signal from one of the delay stages; and

a selecting section, the selecting section comprises a second transistor, a drain of the second transistor is directly connected to the source of the first transistor for activating the buffer section to establish the delay path, wherein

an output signal from the delay path has a desired delay time.

34. (New) A delay circuit comprising:

a delay section having two or more predetermined delay stages, each predetermined delay stage adds a predetermined delay time to an input signal; and

selecting switch sections, at least one of the selecting switch sections comprises:

a buffer section, the buffer section comprises a first transistor, a gate of the first transistor receiving a delayed input signal from one of the delay stages; and

a selecting section, the selecting section comprises a second transistor, a source of the second transistor is directly connected to the drain of the first transistor for activating the buffer section to establish the delay path, wherein

an output signal from the delay path has a desired delay time.